REMARKS

Applicant respectfully requests reconsideration of this application. Claims 20-24 and 40-57 are pending. Claims 20, 40, 42, 49, 50, and 52 have been amended. Claim 44 has been cancelled. No claims have been added.

Therefore, claims 20-24, 40-43, and 45-57 are now presented for examination.

Claim Rejection under 35 U.S.C. §102

Watanabe

The Examiner rejected claims 20-24 and 40-57 under 35 U.S.C. §102 (b) as being anticipated by US Patent No. 5,808,490 of Watanabe (hereinafter "*Watanabe*"). Claim 44 has been cancelled.

Claim 20 of the present application, as modified herein, provides as follows:

20. A bus state keeper comprising:

a plurality of units, each of the units comprising a multiplexer and a flip flop;

wherein each of the multiplexers includes:

a select input, the select input of being coupled with a respective select signal of a plurality of select signals;

an output, the output being coupled to a respective bit of a first bus, the first bus being coupled to a plurality of devices, wherein the first bus is to be kept in a steady state when inactive by the plurality of units,

a first input, the first input being coupled to a respective bit of a second bus, and

a second input,

wherein the second bus is selected as an input by the plurality of multiplexers, and

wherein each of the flip-flops includes:

a data input, the data input coupled to each respective bit of the first bus,

a data output, the data output coupled respectively to the second input of the plurality of multiplexers, and

a clock input, the clock input coupled to a clock signal,

wherein the plurality of flip flops are to store a state of the first bus.

In order to support the rejection under 35 U.S.C. §102 (b), it is necessary that each element of the claim be included in the cited reference, and it is submitted that *Watanabe* does not contain each such element. *Watanabe* does not provide any teaching of a bus state keeper having multiple units, each including a multiplexer and a flip-flop, but rather illustrates a single unit with a single operation. *Watanabe* does not suggest that each of a plurality of multiplexers has a select input that is coupled with a respective select signal of a plurality of select signals. Further, it is submitted that *Watanabe* thus does not include any teaching regarding a second bus that is selected as an input by a plurality of multiplexers.

Watanabe relates to a bus control circuit. As described in the reference, a bus control circuit and an electronic circuit are connected to a bus, and the bus is controlled by storing a signal level that is output to the bus when the bus is in an active state, and fixing the bus to the signal level when the bus switches to an inactive state.

With regard to claim 20, the Examiner largely cites to Figures 2A and 3 and the related text of *Watanabe*. Figure 2A illustrates a bus control circuit 1 that includes a latch 1a and a switch 1b. It is submitted initially that Figure 2A is distinguishable in that it includes a switch instead of a multiplexer, which are different devices. In this illustrated circuit, the latch provides one of the inputs to the switch, with an "out" signal

providing the other input. However, it is noted that the switch is controlled by a bus control signal. "The latch unit 1a has a control terminal which receives a bus control signal, which enables and disables the latch unit 1a. The bus control signal is supplied from the device related to the bus control circuit 1 or one of the circuits 3a and 3b." (*Watanabe*, col. 3, lines 56-62) Thus, the effect of the bus control unit is to either enable or disable the latch. This is essentially an ON or OFF state for the use of the latches. "The switch unit 1b has a second stationary contact, which receives an output signal OUT to be transferred over the bus 2, and a movable contact which is selectively connected to are [one?] of the first and second stationary contacts in response to the bus control signal applied to the control terminal of the switch unit 1b." (*Watanabe*, col. 3, lines 62-67)

The application of the system shown in Figure 2A is further illustrated in Figure 3, which is described as follows:

> FIG. 3 is a block diagram of a bus control circuit according to a first embodiment of the present invention based on the structure shown in FIG. 2A. A bus control circuit 21 is connected to a bus 22 to which circuits 23a, 23b and 23c are connected. The bus control circuit 21 includes an input/output buffer 21a, a through latch (also referred to as a level latch) circuit 21b, a multiplexer (MUX) 21c and an AND gate 21d.

(*Watanabe*, col. 5, lines 4-11)

As shown in Figure 3 of *Watanabe*, the circuit includes a latch and a multiplexer. The input and the output of the latch are connected to an input/output buffer 21a, and a signal input to the latch, which would appear to be a clock signal input, is connected to a four-input AND gate 21d.

As this is explained in *Watanabe*:

Turning to FIG. 3 again, the through latch circuit 21b is in the through state when a control signal *G applied thereto is low, and is in the hold state when the control signal *G is high. The through latch circuit 21b allows the input signal from the input/output buffer 21a to pass through the multiplexer 21c in the through state, and latches the input signal in the hold state. The multiplexer 21c is controlled by an output control signal *0 output by a related part of the internal circuit 32 shown in FIG. 4. When the output control signal *0 is at the low level, the multiplexer 21c selects an output signal OUT output by a related part of the internal circuit 32. When the output control signal *0 is at the high level, the multiplexer 21c selects the output signal of the through latch circuit 21b. The AND gate 21d receives the above-mentioned output control signal *0 and output control signals *1, *2 and *3 respectively output by circuits 23a, 23b and 23c which are, for example, LSI devices such as memory devices. The circuits 23a, 23b and 23c output low-level such output control signals when the circuits are in the output states, and output high-level such output control signals when the circuits are in the input states. It will be noted that only one of the circuits 23a, 23b and 23c switches to the output state at one time. The AND gate 21d derives the control signal *G.

(*Watanabe*, col. 5, lines 39-62) (emphasis added) Thus, the latch receives a clock signal that is produced by ANDing the output of multiple circuits on the bus with output control signal *0. The multiplexer is enabled by output control signal *0.

Watanabe is illustrating a system that is enabled by a control line, with a latch that is clocked by the combination of multiple inputs. There is no teaching of the use of plurality of units, with each unit having a multiplexer and a flip-flop. Even if it is assumed for the sake of argument that multiple multiplexers were in fact utilized in *Watanabe*, there is not suggestion that each multiplexer has a select input to be coupled

with a respective select signal of a plurality of select signals. *Watanabe* illustrates a single output control signal *0. Again assuming for the sake of argument that multiple multiplexers are utilized in *Watanabe*, the reference further does not teach a bus that is selected as an input by the plurality of multiplexers.

Thus, *Watanabe* does not contain each of the elements of the claims. It is respectfully submitted that the claims are allowable, and the Applicant requests that the rejection of the claims be removed.

It is submitted that the above arguments also apply to independent claims 40, 45, and 50, and thus such claims are also allowable. The remaining claims are dependent claims, and are allowable as being dependent on the allowable base claim.

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (503) 439-8778 if there remains any issue with allowance of the case.

Request for an Extension of Time

The Applicant respectfully petitions for a one-month extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a). A check is enclosed for the fee for such extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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